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Design and Implementation Of Packet Switched Network Based RKT-NoC on FPGA

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ABSTRACT
In this Paper we proposed a new network on chip that handles accurate localization of the faulty parts of NoC. The proposed NoC is based on new error detection mechanism and modified xy routing algorithm. Error detection mechanism suitable for dynamic NoCs, where the number and position of the processor elements or faulty blocks vary during run time. This paper also presents a modified xy routing algorithm combined with a scheduler to be used on NoCs.This proposed method is fast way to transferring data via specific path between two nodes in the network and the scheduler further helps to avoid collision. More latency and fewer throughputs are obtained with contentation in network. As mesh size increases latency and throughputs increases accordingly. The proposed design implemented in SPARTAN III FPGA by using Xilinx ISE13.4and simulated in Questa sim 10.0b.
Keywords – Network on Chip, Modified xy Routing algorithm, Dynamic Reconfiguration

I. INTRODUCTION

Recently the trend of embedded system has been moving toward multiprocessor system-on-chip (MPSoCs) in order to meet the requirements of real-time application. The complexity of these SoCs is increasing and the communication medium is becoming a major issue of the MPSoCs [1].Generally integrating a network- on-chip (NoC) into the SoC provides an efficient means to interconnect several processor elements (PEs) or intellectual properties(IP)[2].Network on-chip is slowly being accepted as an important paradigm for implementation among various cores in a soc.

With advances in integrated circuits(IC) manufacturing a constant attempt has been to design enormous amounts of networks on the same chip so as tocomplish more networks embedded on the chip.Figure1shows the conceptual view of a NoC where each tile is composed of a resource(R) and a switch or router(s).The routers are connected to the four neighboring tiles and its local resource via channels. Each channel consists of two directional point to point links between two routers or a router and a local resource. Traditionally, System-on-chip (SoC) utilizes topologies based on shared buses [3]. According to NoC design approach designers use network design technology to analyze and design SoCs .In other words designers view a SoC as a micro-network of components. SoC interconnection design can be done using the micro network stack paradigm, which is an adaptation of the protocol stack. NoC can be defined as "network on chip is a communication network targeted for on chip".For the NoC architecture, the chip is divided into a set of interconnected blocks where each node can be a general purpose processor like a digital signal processing element (PE).

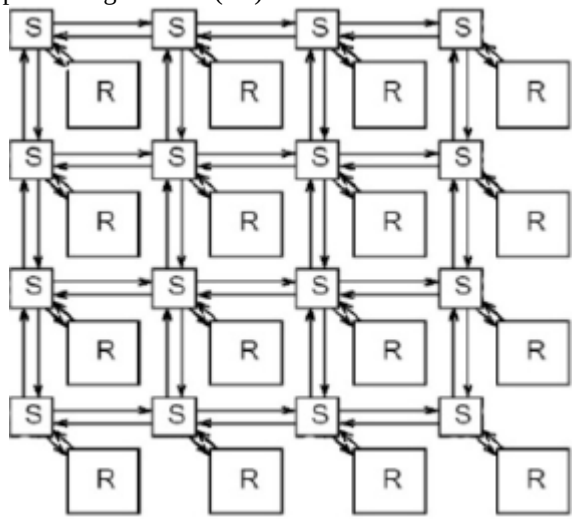

Figure1: Structure of 4X4 NoC

A router is embedded within each node with the objective of connecting it to its neighboring nodes. The router has four ports(west,south,East and north) to connect with the other routers and a local port to connect with PE means have five ports input and five output ports as shown in figure2.

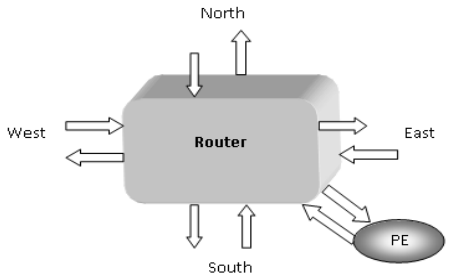

Figure: 2 Generic structure of router.

In this paper, we present a new reliable dynamic NoC.

The proposed NoC is a mesh structure of routers able to detect routing errors for adaptive routing based on modified xy routing algorithm. Our approach includes data packet error detection and correction. The originality of the proposed architecture is its ability to localize accurately error sources, allowing the throughput and network load of the NoC to be maintained.

II. Existing Method

The RKT-NoC is a packet switched network based on intelligent independent reliable routers called RKT-switches [4].The architecture of the RKT-switch is depicted in figure3.The RKT-switch is characterized by its architecture having four directions (north, east, south and west) suitable for a 2-D mesh NoC. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP .The RKT-switch operation is based on the store-and-forward switching technique.

This technique is suitable fo dynamicallyreconfigurable NoCs. Indeed, in our NoC PEs and IPs can be implemented in place of one or several routers. In store and forward technique ,each data packet is stored is stored only in a single router .Hence, when router needs to be reconfigured the router is only required to empty its buffers.

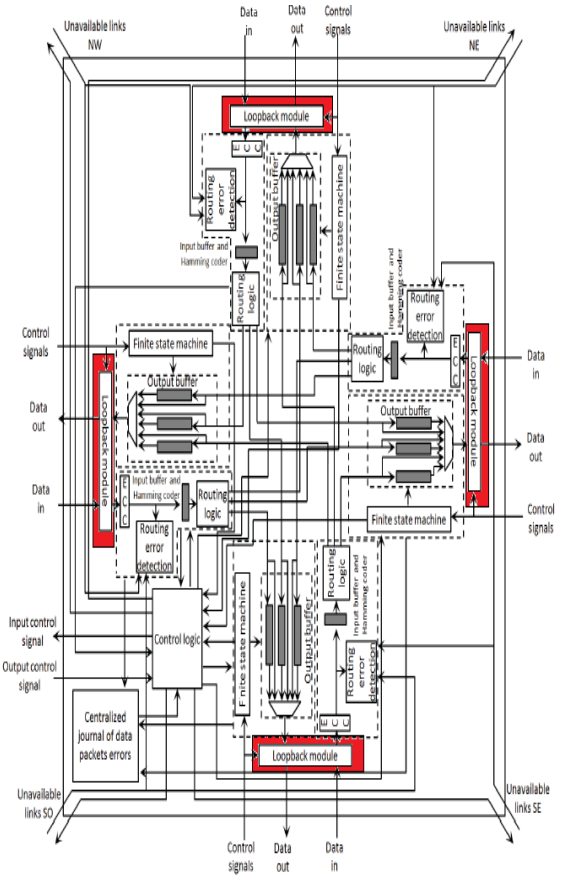

Figure3: Architecture of reliable route RKT-NoC

III. Proposed Method

We proposed a new reliable NoC-based communication approach called RKT-NoC. The reliable switch being proposed incorporates an online routing fault detection mechanism based on modified XY-routing algorithm [5].The hamming ECC is considered for our RKT-switch, in order to provide a convenient tradeoff between area overhead and error correction capacity [6].This choice permits the correction of single event upset(SEU)errors and the detection of multiple event upset errors(MEU)errors. An modified XY-based adaptive algorithm primarily uses the rules of the XY algorithm to route data packets into the network when the required components are available in case of an unavailable component, a specific routing path is locally chosen to bypass its position.

When a router receives a data packet, it checks the correctness made by the routing .Decision of the previous node, using the routing error detection algorithm.

From address comparison, the router checks if the previous routing decision obeyed the XY routing algorithm. If the router in the XY path is unavailable, the previous router decision was a correct bypass. If it is available, the previous router decision is a routing error.

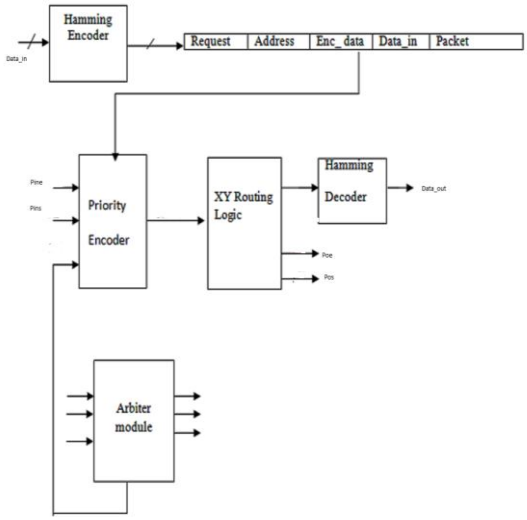

Figure4: Methodolgy of Router1

In the latter case, the router adds one "1"to the error journal associated with the faulty routing logic block. If three consecutive errors are performed by the same faulty routing logic block, a permanent error is considered. In this

Situation, a specific data packet is generated towards the switch generating the routing errors. This specific one-flit data packet indicates the faulty input ports of the considered router that must be disconnected. For NoCs based on multiflit data packets as shown in table1, it may happen that a flit is received without being preceded by a header flit. In the proposed RKT-NoC, there is bit in each flit indicating whether the flit is header flit or a data flit, as shown in table I.

When router receives first flit of a data packet, it checks after the hamming decoding whether it is a header flit. If not, the flit is destroyed. Therefore, when receiving a data packet, the destination IP or PE counts the number of received flits. If this number does not match the number in indicated in the header flit, the packet is destroyed and retransmission request is sent back to the emitter IP or PE.In the proposed method we have taken 4x4routers a shown in Figure1.

In the Block diagram of router1as shown in figure4 input data is first encoded.

After packet generation based on priority encoder it is applied to routing logic. The proposed diagram uses modified xy routing algorithm combined with scheduler to be used on NoCs. The same methodology can be applied to all sixteen routers. All packet having Req bit is undergoes for the modified XY routing algorithm depends upon the priority given by arbiter. Packet is store in FIFO unstill its get grand signal from arbiter. Once get grand signal actual XY Routing takes place.

IV. EXPERIMENTAL RESULTS

By simulation and synthesis the following results are obtained for each cycle with different nodes for different input data. Here Xilinx 12.2_1 tool is used in order to synthesize and simulate the design process and also the netlist generation.

A. Simulation Result

The following figure shows the simulation results for different inputs and outputs for different nodes.

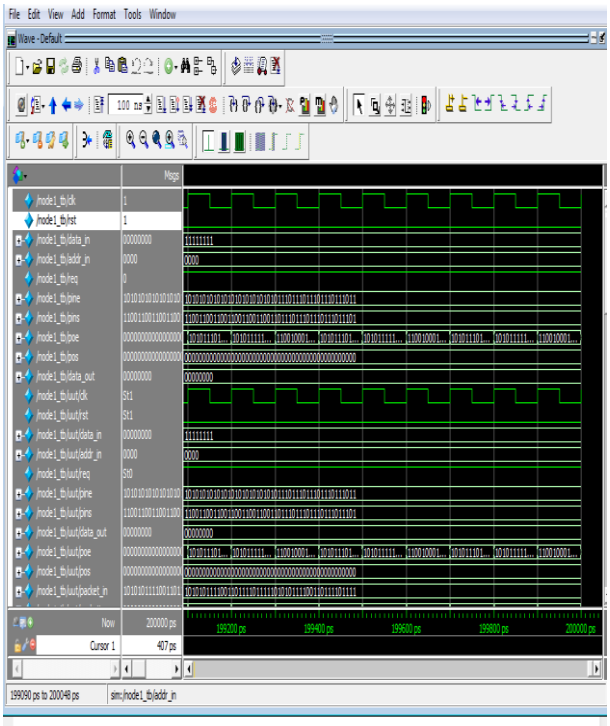

Figure: A simulation result Node1.

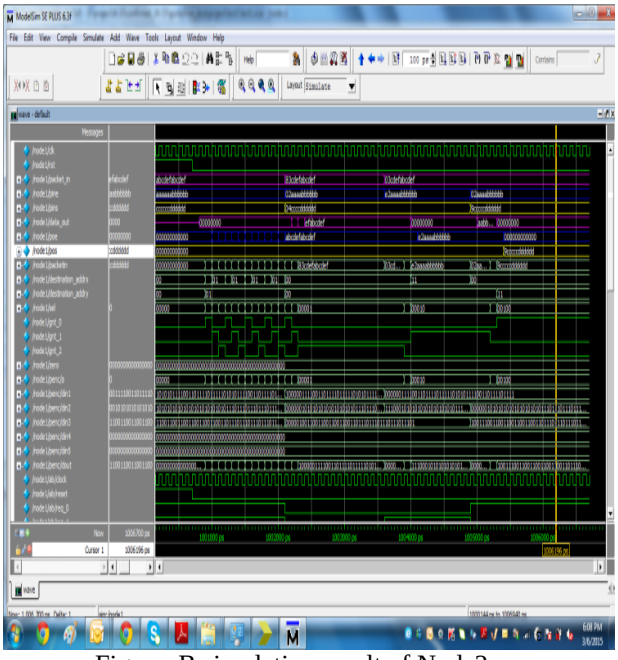

Figure: B simulation result of Node2

B. Synthesis Result

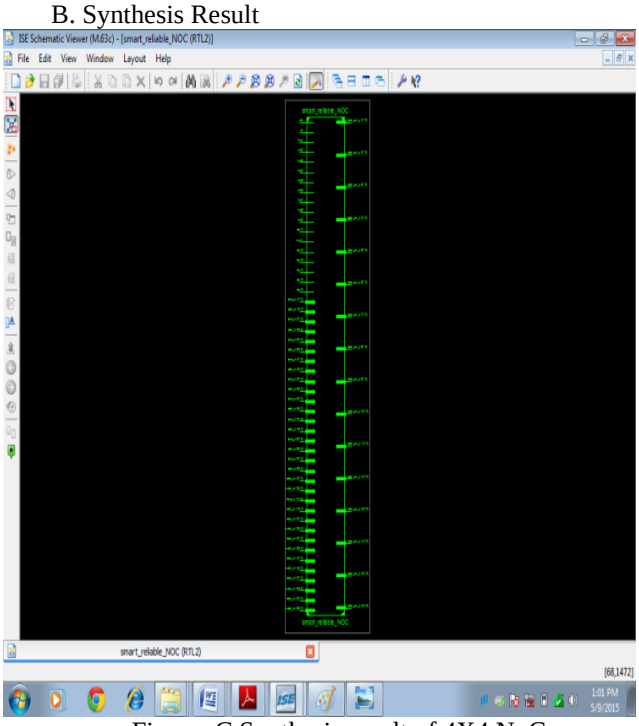

Figure: C Synthesis result of 4X4 NoC

V. CONCLUSION

In the paper, we proposed error correction and detection method for dynamically reconfigurable NoCs. The proposed method also presents a modified XY routing algorithm combined with scheduler to be used on NoCs. The results shows that the proposed method is fast and an efficient way to transferring a data via a specific path between two nodes in the network and the scheduler further helps to avoid collision .It requires smaller memory and more latency and fewer throughputs are obtained with contentation in network.

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